FIG. 1A

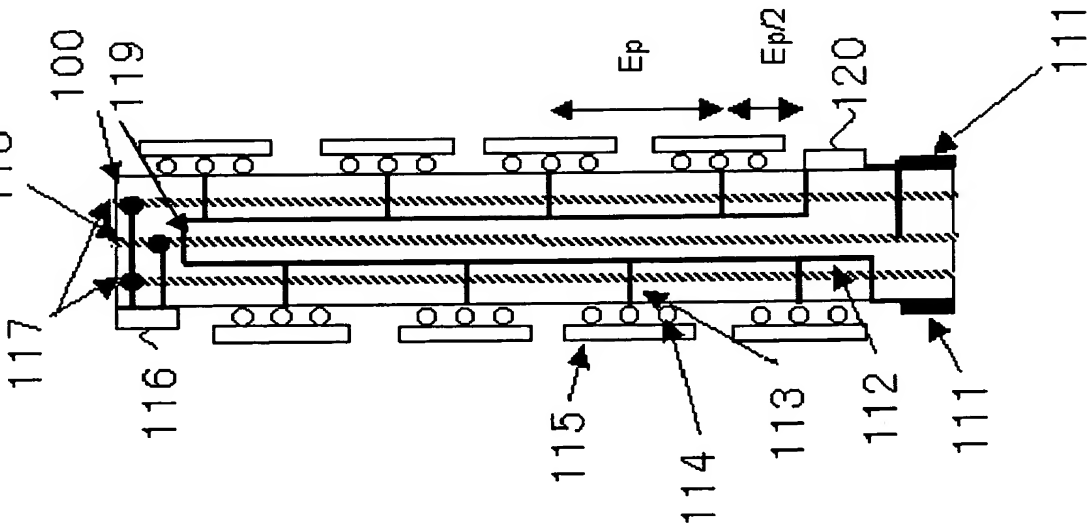

118
100
119
117
116
115
114
113
112
111
Ep
Ep/2
120

FIG. 1B

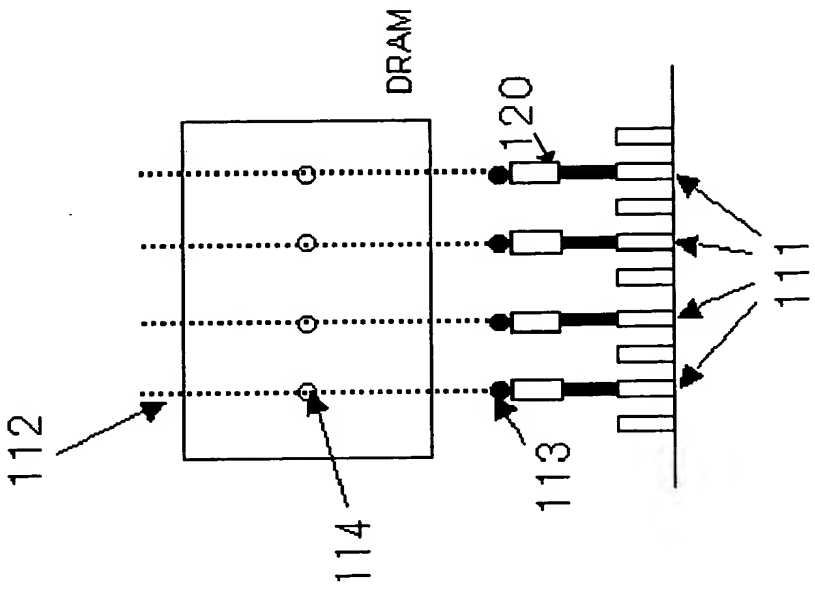
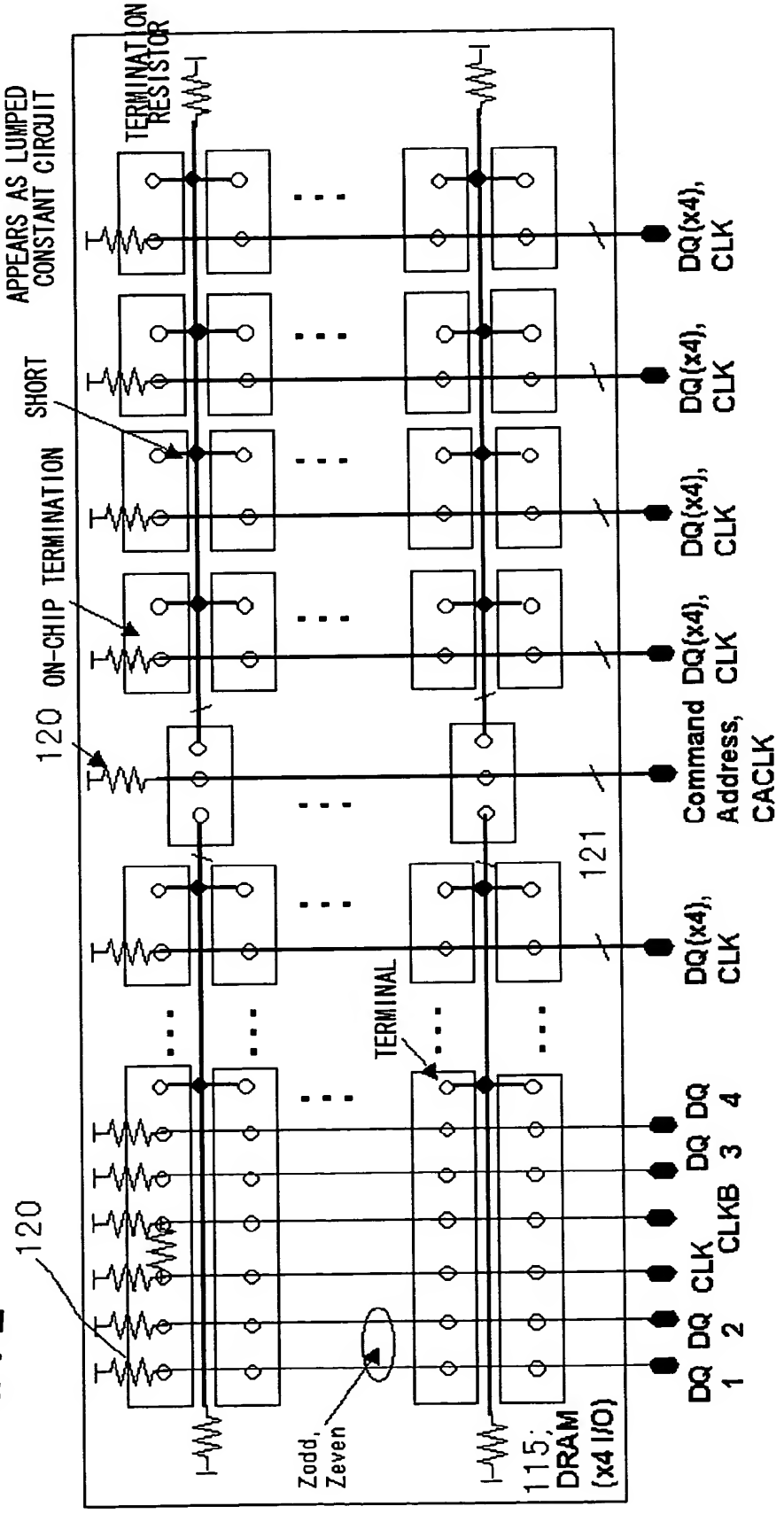

DRAM
120
111
112
114
113

FIG. 2


120
APPEARS AS LUMPED CONSTANT CIRCUIT
TERMINATION RESISTOR
SHORT
120 ON-CHIP TERMINATION
TERMINAL
121
Zodd, Zeven
115; DRAM (x4 I/O)
DQ 1
DQ 2
CLK
CLKB
DQ 3
DQ 4
DQ(x4), CLK
Command Address, CACLK

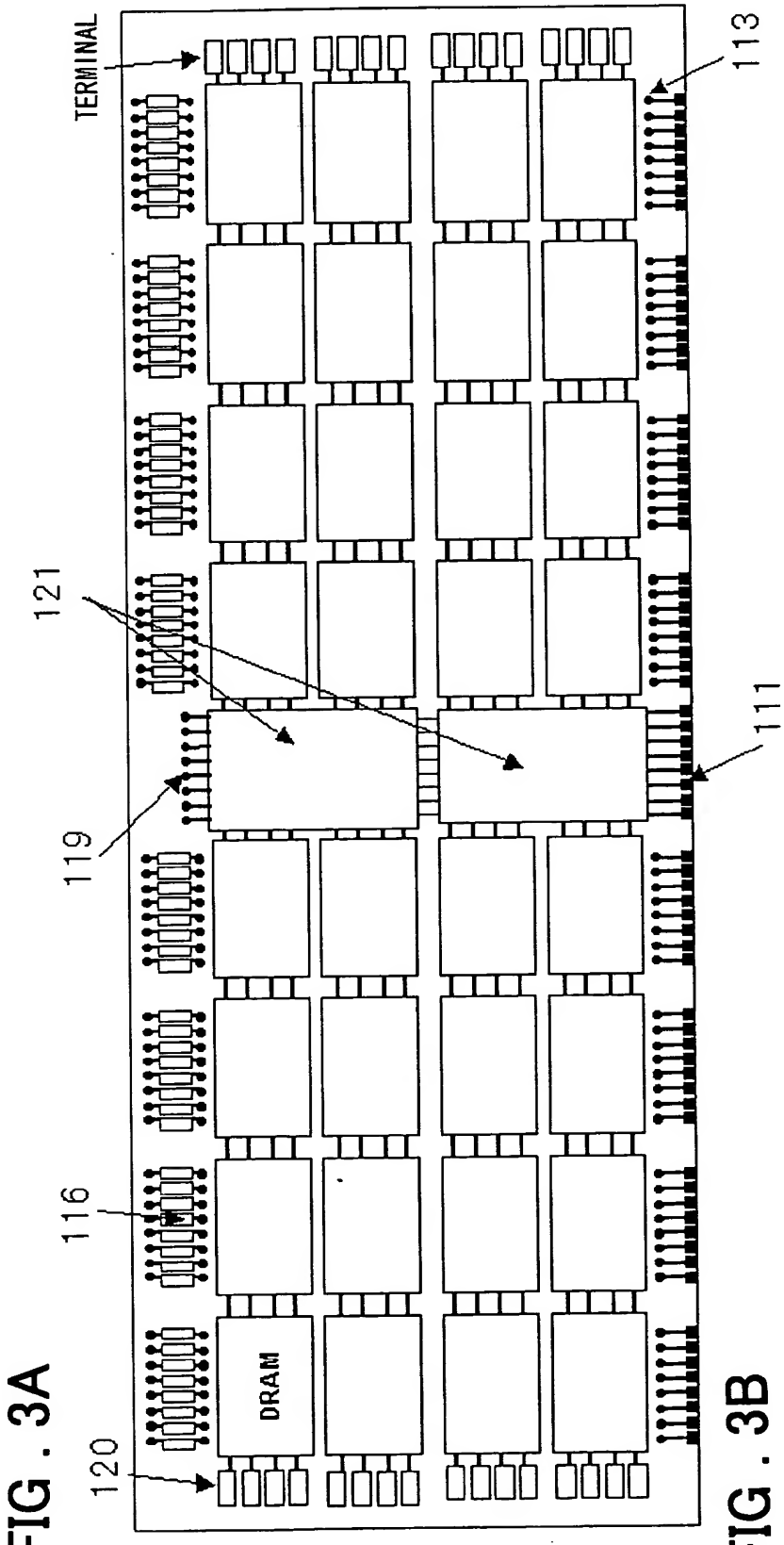

TERMINAL
113
121
111
119
116
DRAM
120

FIG. 3A

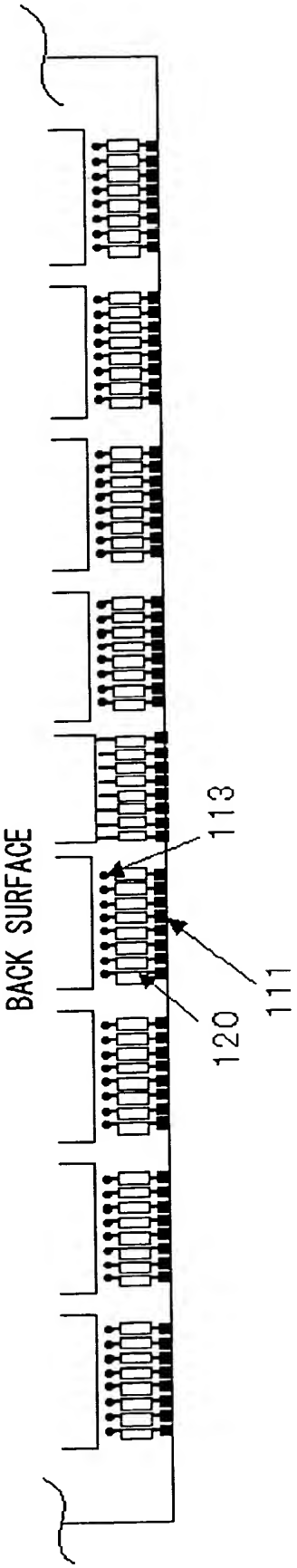

BACK SURFACE
113
111
120

FIG. 3B

FIG. 4A

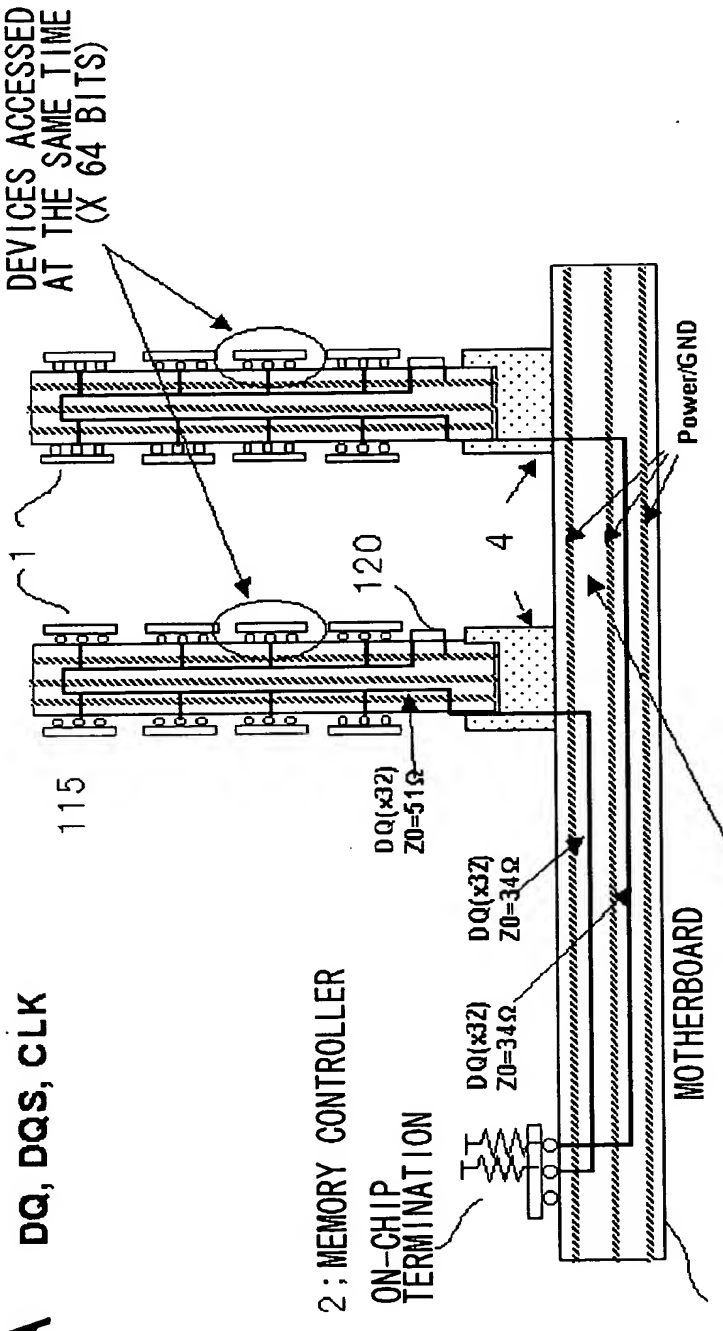

DEVICES ACCESSED
AT THE SAME TIME
(X 64 BITS)
1
115
120
4
DQ(x32)
Z0=51Ω
DQ(x32)
Z0=34Ω
DQ(x32)
Z0=34Ω
2 ; MEMORY CONTROLLER
ON-CHIP
TERMINATION
MOTHERBOARD
Power/GND
3
Command/Address
T-branch

FIG. 4B

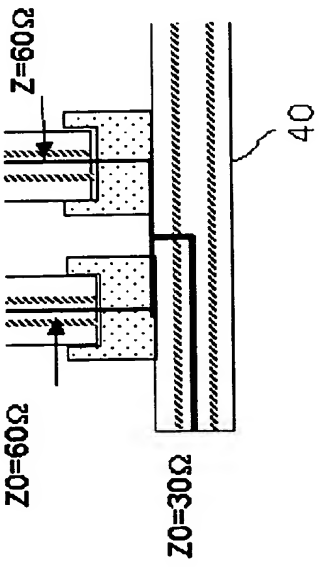

Z=60Ω
Z0=60Ω
Z0=30Ω
40

FIG. 5

DQ@WRITE: LATCH BY CLK (CENTER ALIGNED)
DQ@READ: LATCH BY DQS (CENTER ALIGNED)
CA@REGISTER: LATCH BY CACLK
CA@DRAM: LATCH BY CLK

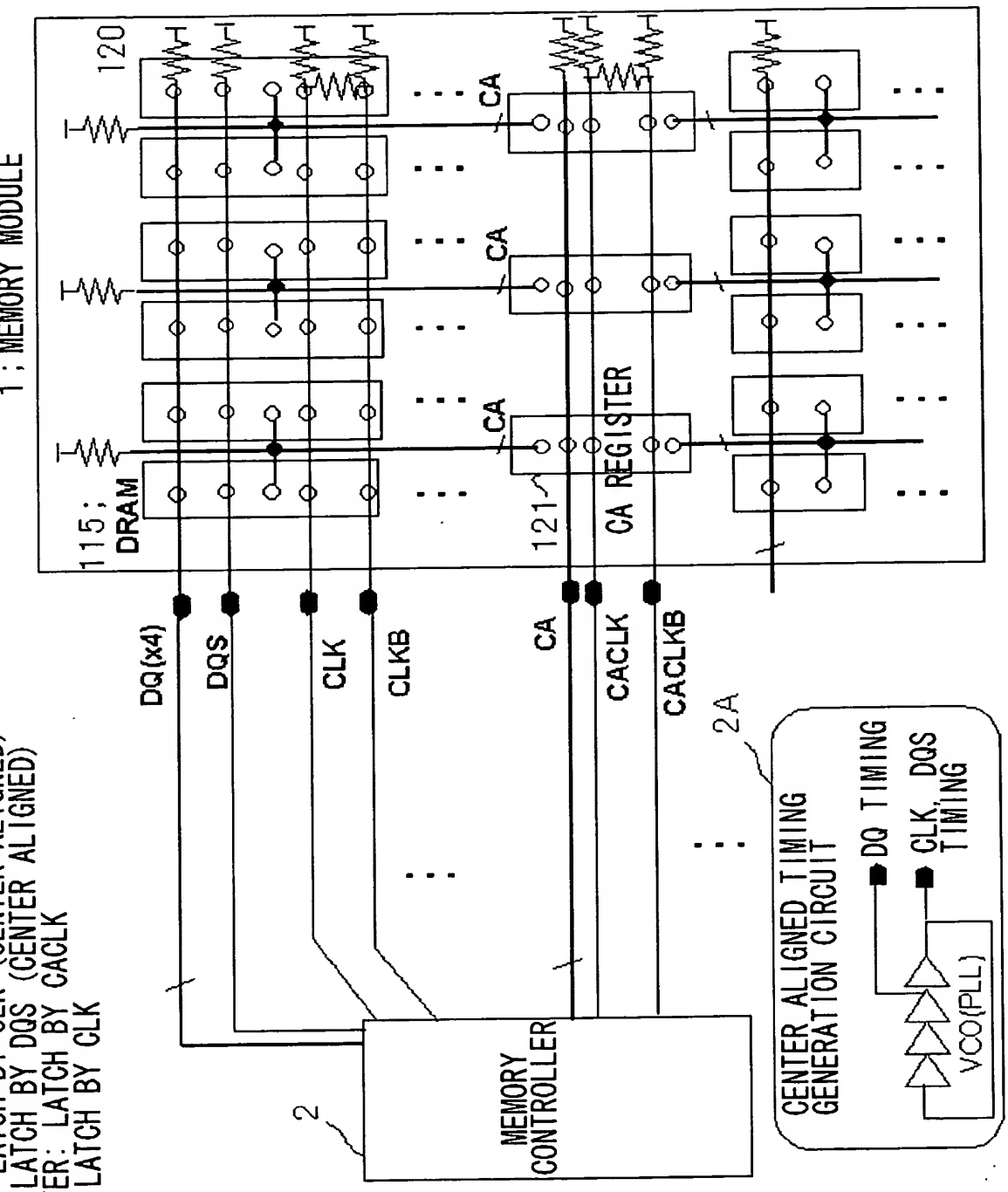


FIG. 6A

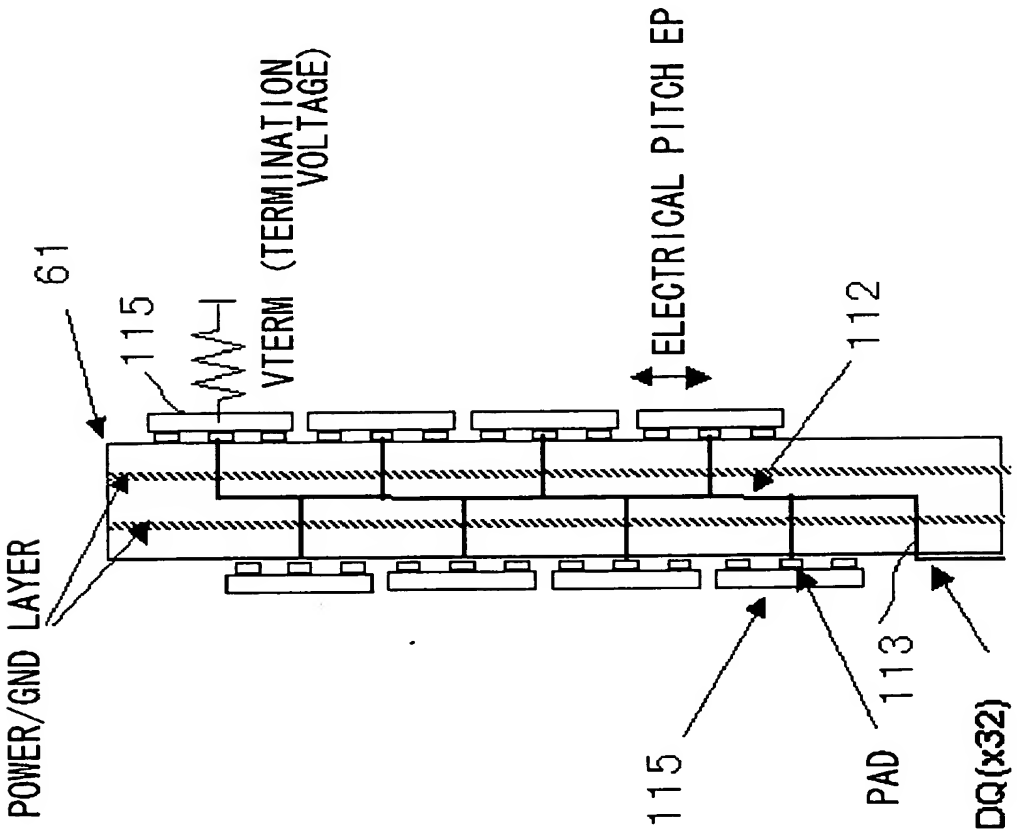
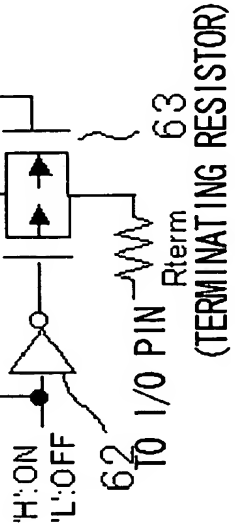

POWER/GND LAYER
61
115
VTERM (TERMINATION VOLTAGE)
ELECTRICAL PITCH EP
112
115
PAD
113
DQ(x32)

FIG. 6B


ON-CHIP TERMINATOR
Vterm
'H':ON
'L':OFF
62
TO I/O PIN
Rterm
(TERMINATING RESISTOR)
63

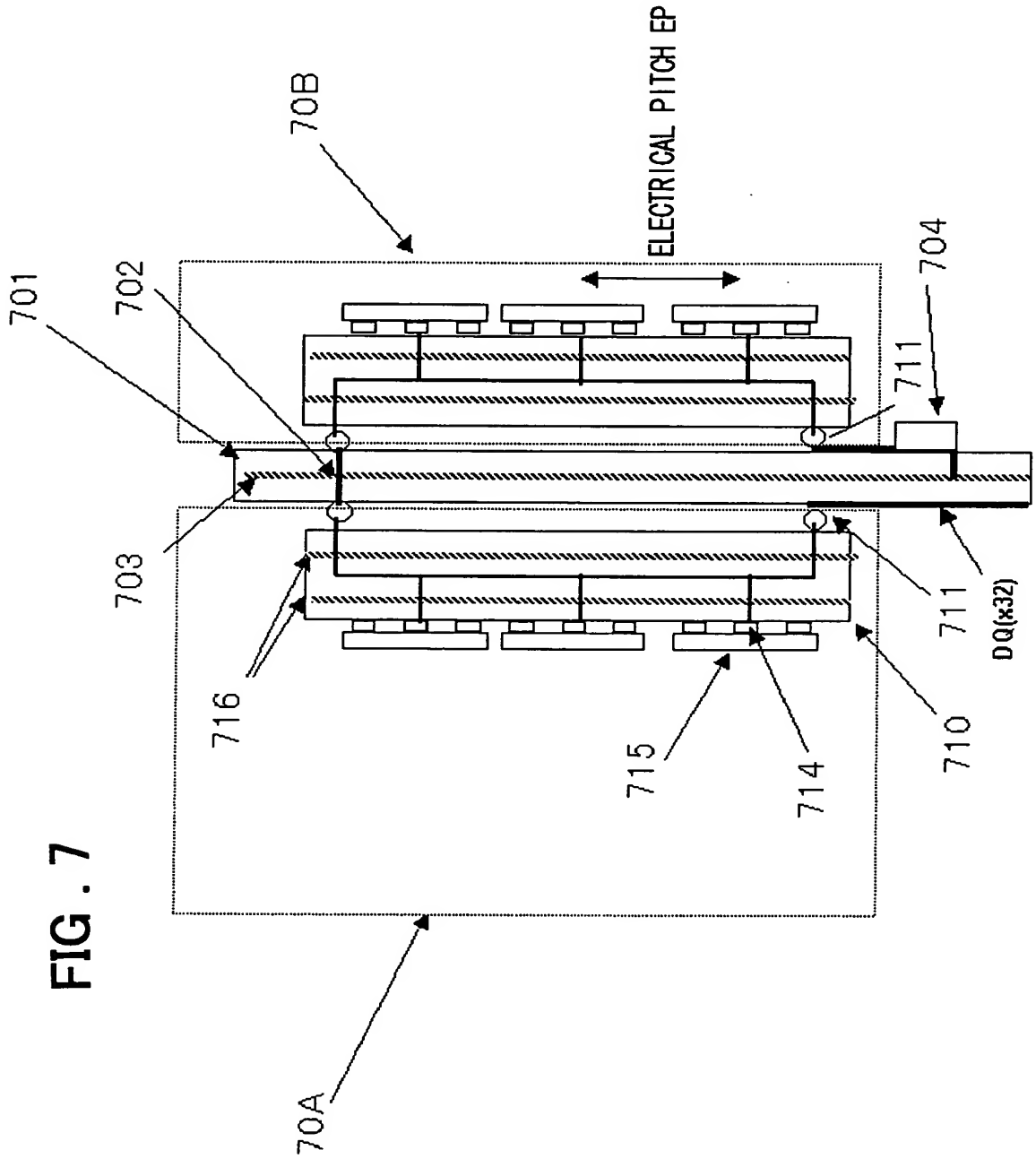

70B
ELECTRICAL PITCH EP
701
702
704
711
703
716
715
714
710
711
DQ(x32)
70A

FIG. 7

FIG. 8A

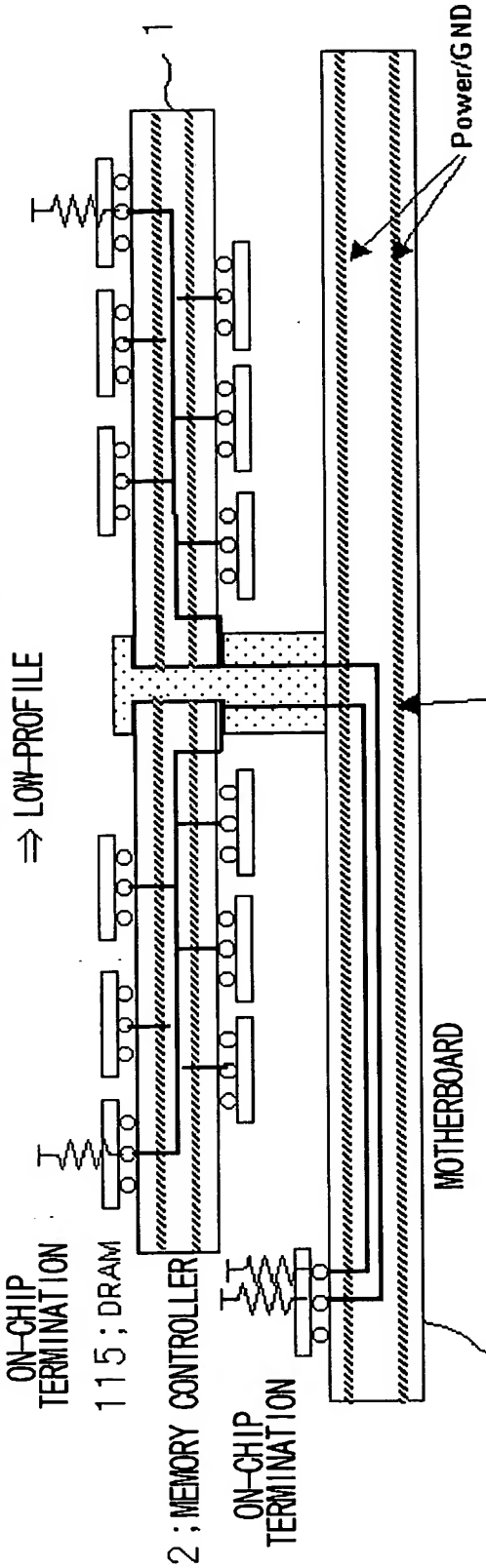

DQ, DQS, CLK
4B ; BUTTERFLY CONNECTOR
⇒ LOW-PROFILE
1
Power/GND
ON-CHIP TERMINATION
115 ; DRAM
2 ; MEMORY CONTROLLER
ON-CHIP TERMINATION
MOTHERBOARD
3

FIG. 8B

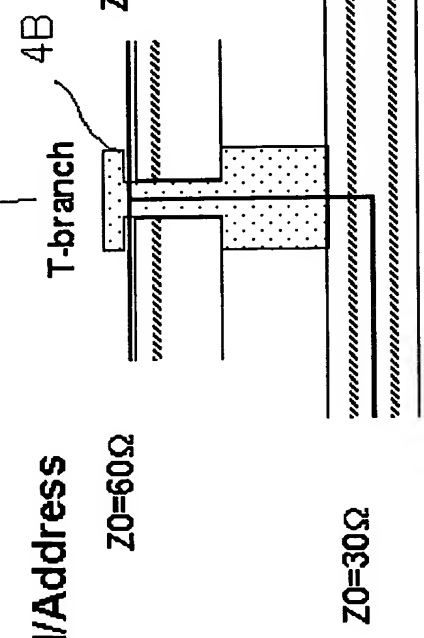

Command/Address
T-branch
4B
Z0=60Ω
Z0=60Ω
Z0=30Ω

FIG . 9

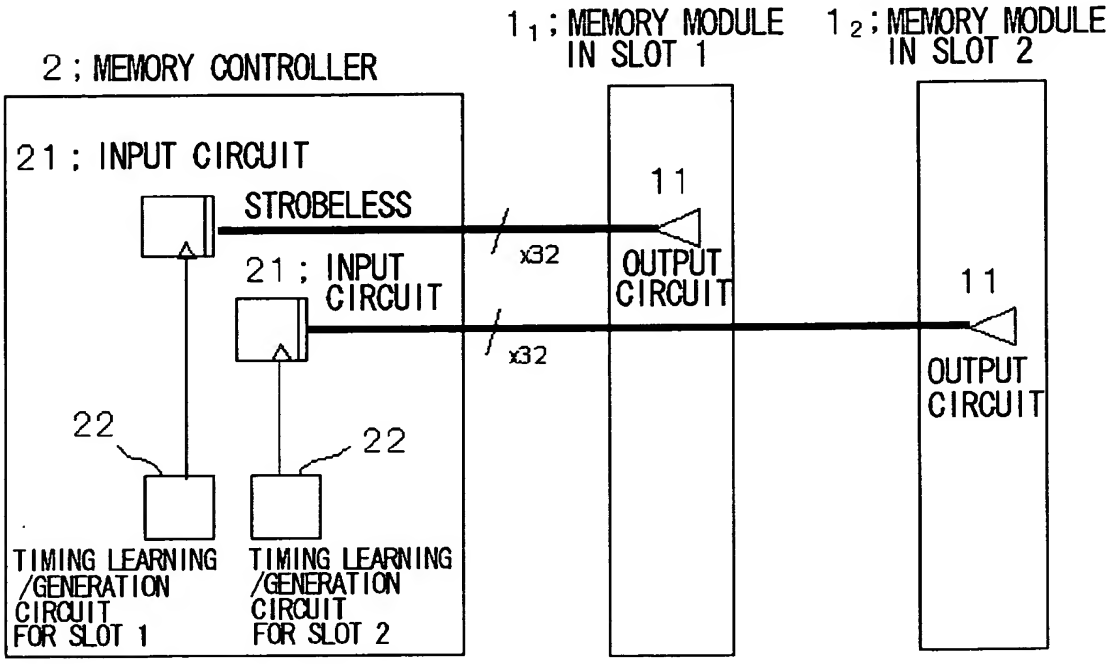

1 1 ; MEMORY MODULE IN SLOT 1
1 2 ; MEMORY MODULE IN SLOT 2
2 ; MEMORY CONTROLLER
21 ; INPUT CIRCUIT
STROBELESS
21 ; INPUT CIRCUIT
x32
x32
11
OUTPUT CIRCUIT
11
OUTPUT CIRCUIT
22
22
TIMING LEARNING /GENERATION CIRCUIT FOR SLOT 1
TIMING LEARNING /GENERATION CIRCUIT FOR SLOT 2

FIG . 10

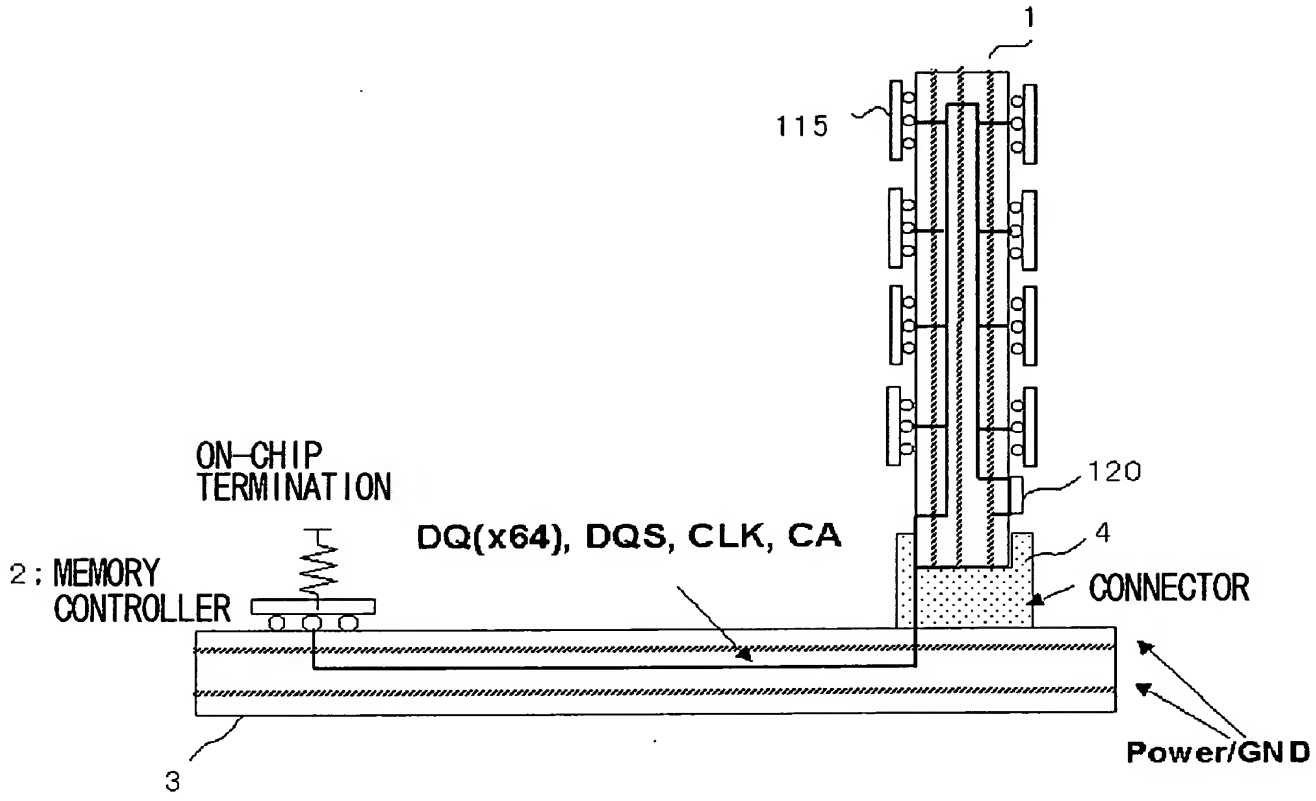

1
115
ON-CHIP
TERMINATION
120
DQ(x64), DQS, CLK, CA
4
2 : MEMORY
CONTROLLER
CONNECTOR
3
Power/GND

FIG . 11A

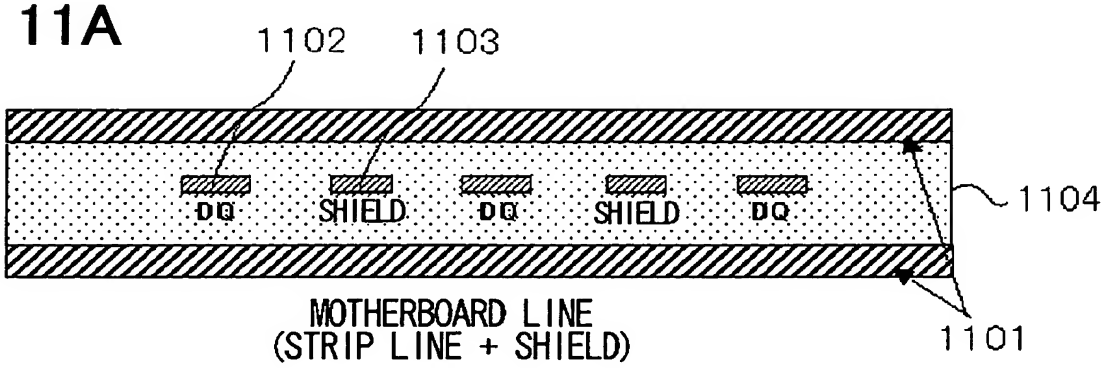


FIG . 11B

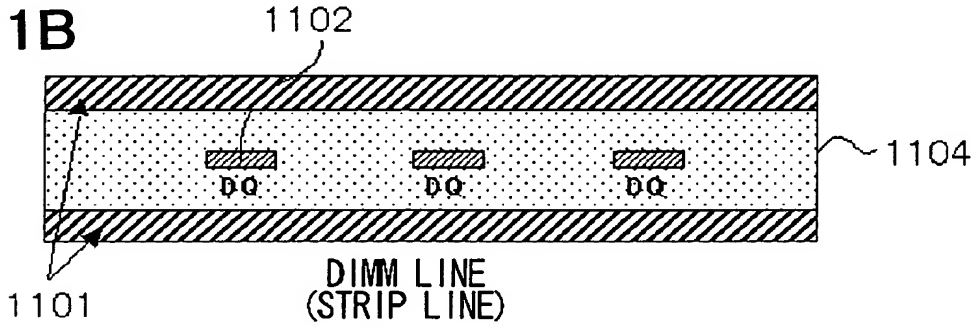


FIG. 12

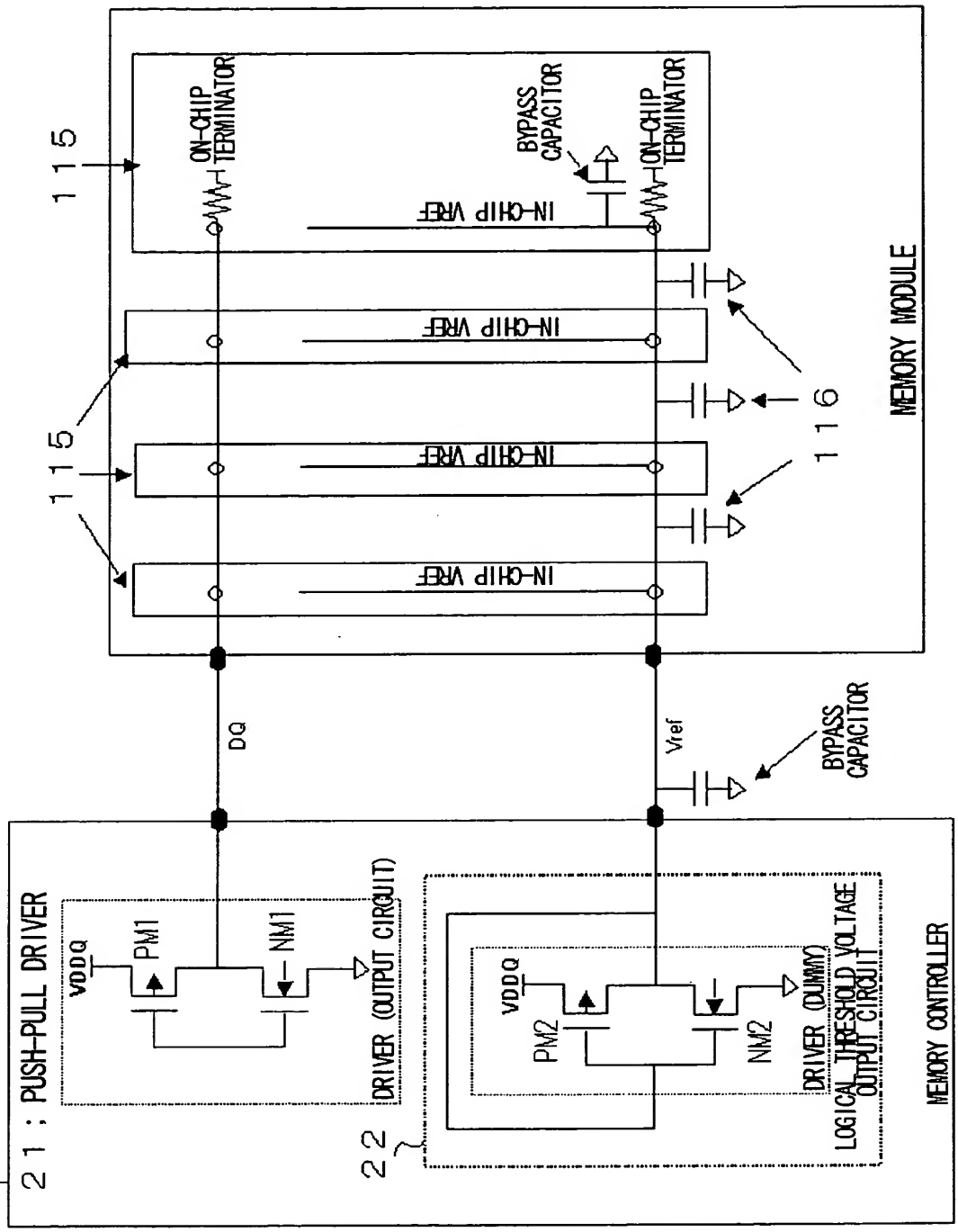

2
21 : PUSH-PULL DRIVER
VDDQ
PM1
NM1
DRIVER (OUTPUT CIRCUIT)
22
VDDQ
PM2
NM2
DRIVER (DUMMY)
LOGICAL THRESHOLD VOLTAGE OUTPUT CIRCUIT
MEMORY CONTROLLER
DQ
Vref
BYPASS CAPACITOR
115
ON-CHIP TERMINATOR
BYPASS CAPACITOR
ON-CHIP TERMINATOR
IN-CHIP VREF
IN-CHIP VREF
IN-CHIP VREF
IN-CHIP VREF
115
116
MEMORY MODULE

FIG . 13A

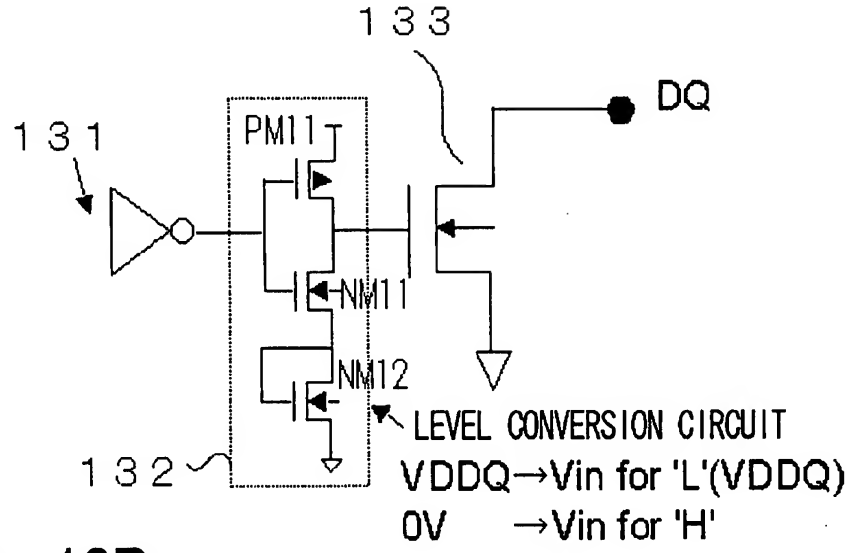


FIG . 13B

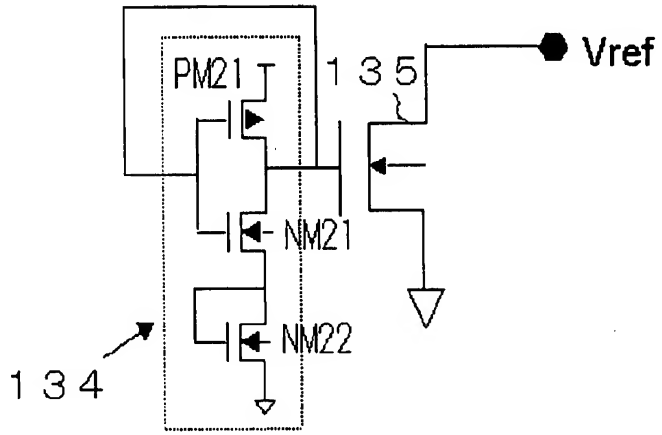


FIG . 13C

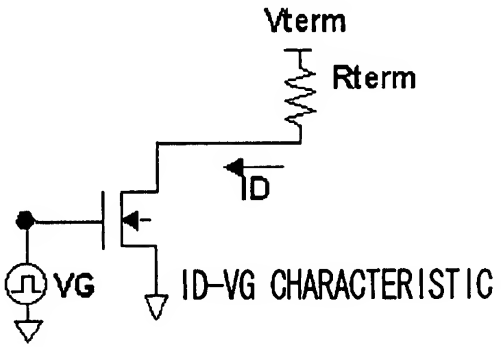
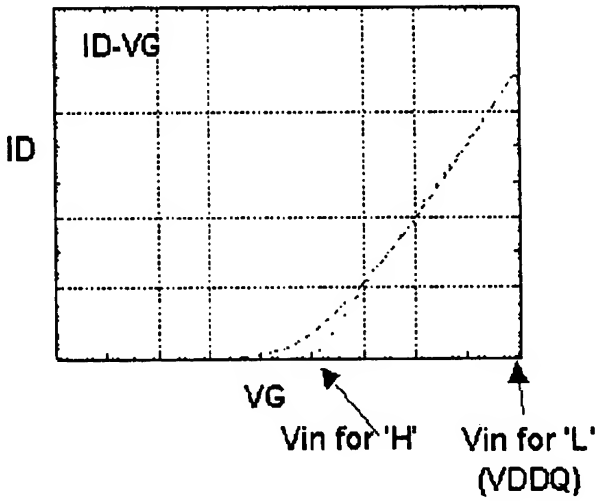


FIG . 13D



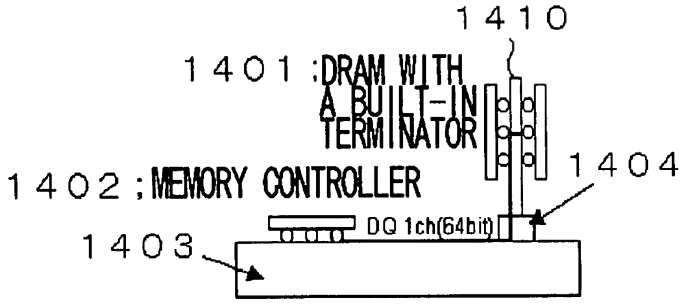


FIG . 14a Point to Point

PRIOR ART

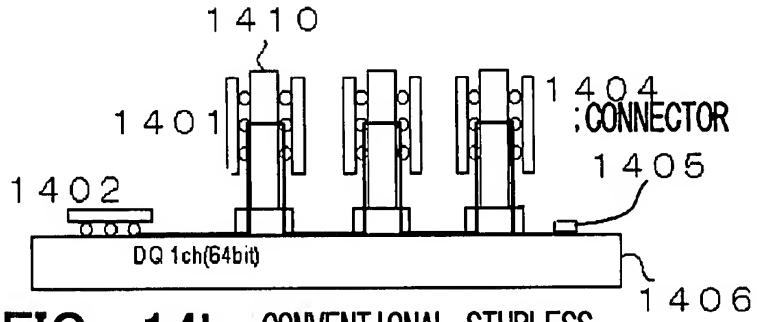


FIG . 14b CONVENTIONAL STUBLESS CONFIGURATION

PRIOR ART

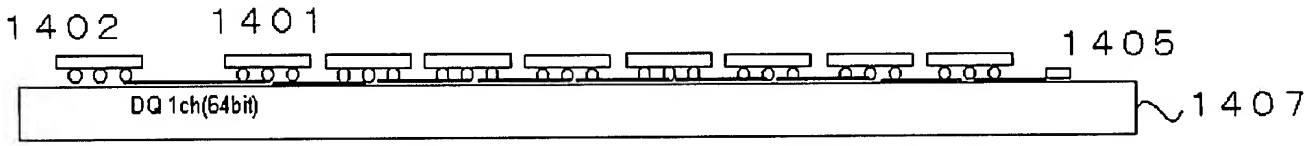


FIG . 14c DIRECT STUBLESS CONFIGURATION

PRIOR ART

FIG. 15A

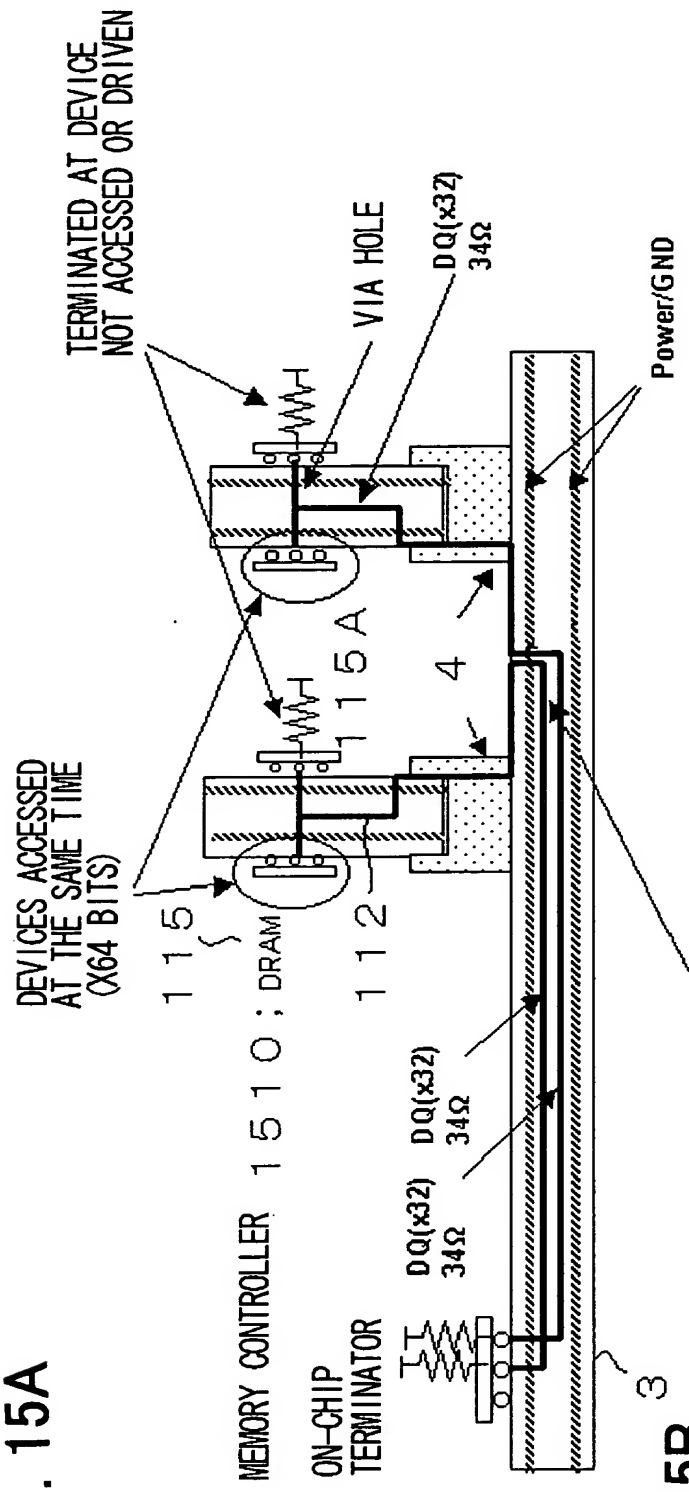


FIG. 15B

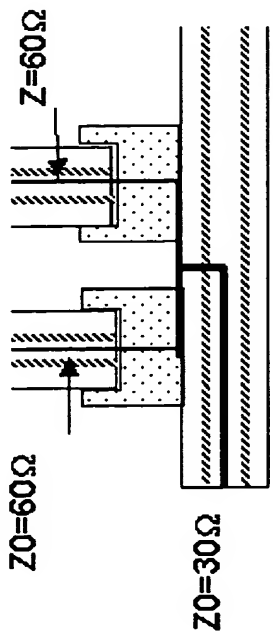


FIG. 16A

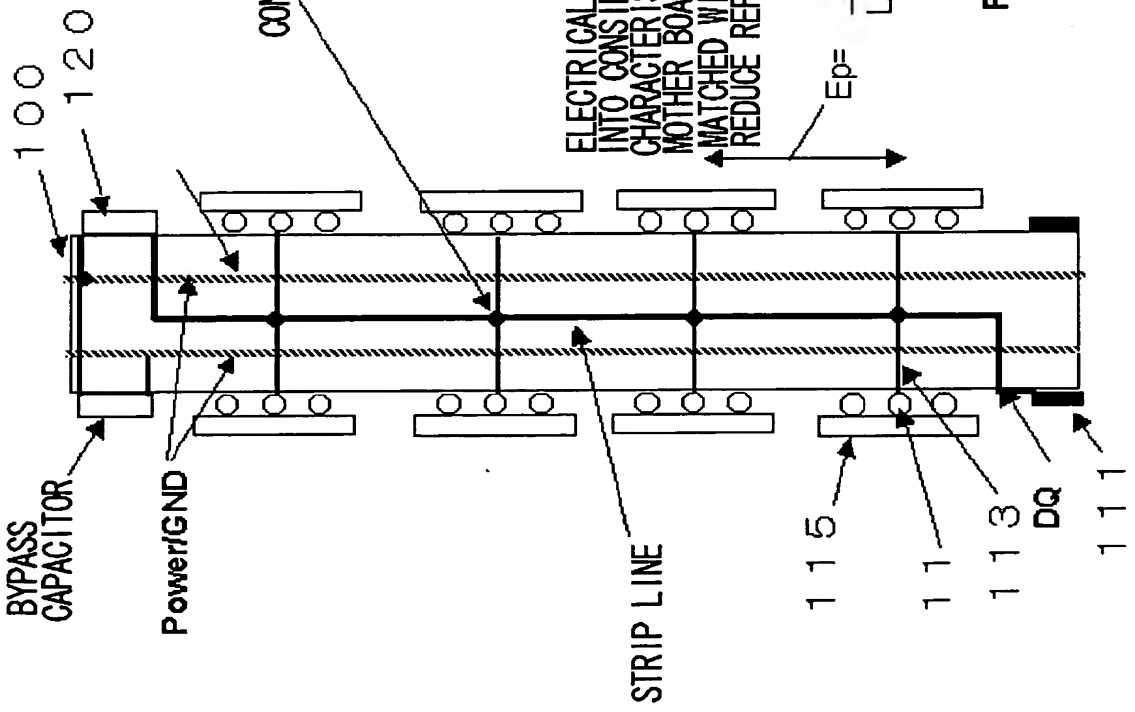


FIG. 16B

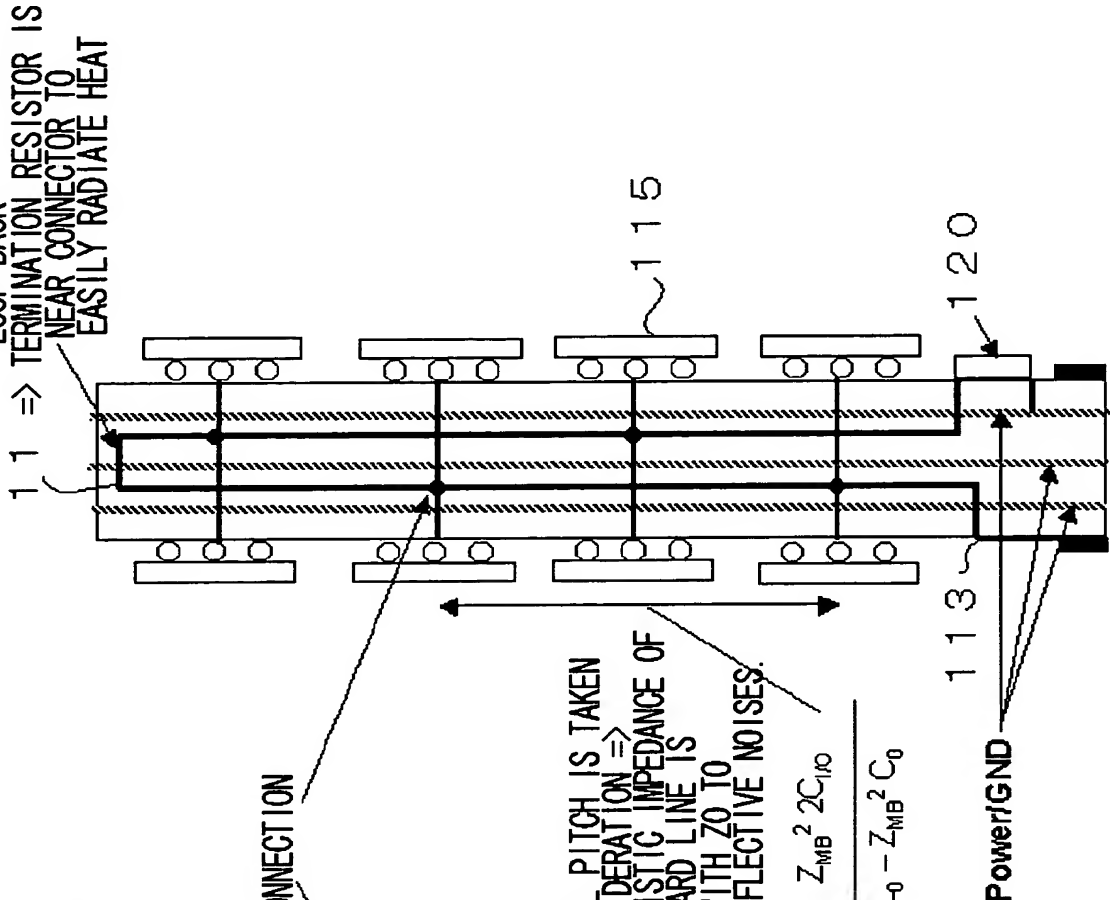


FIG . 17

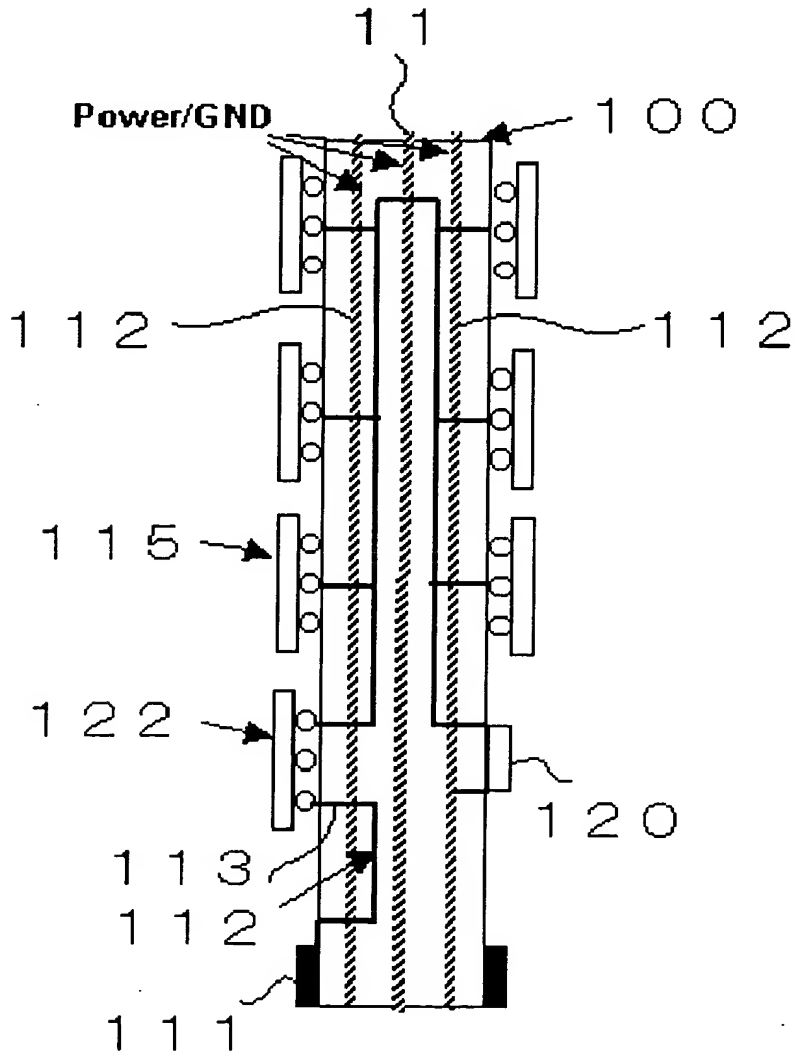


FIG . 18

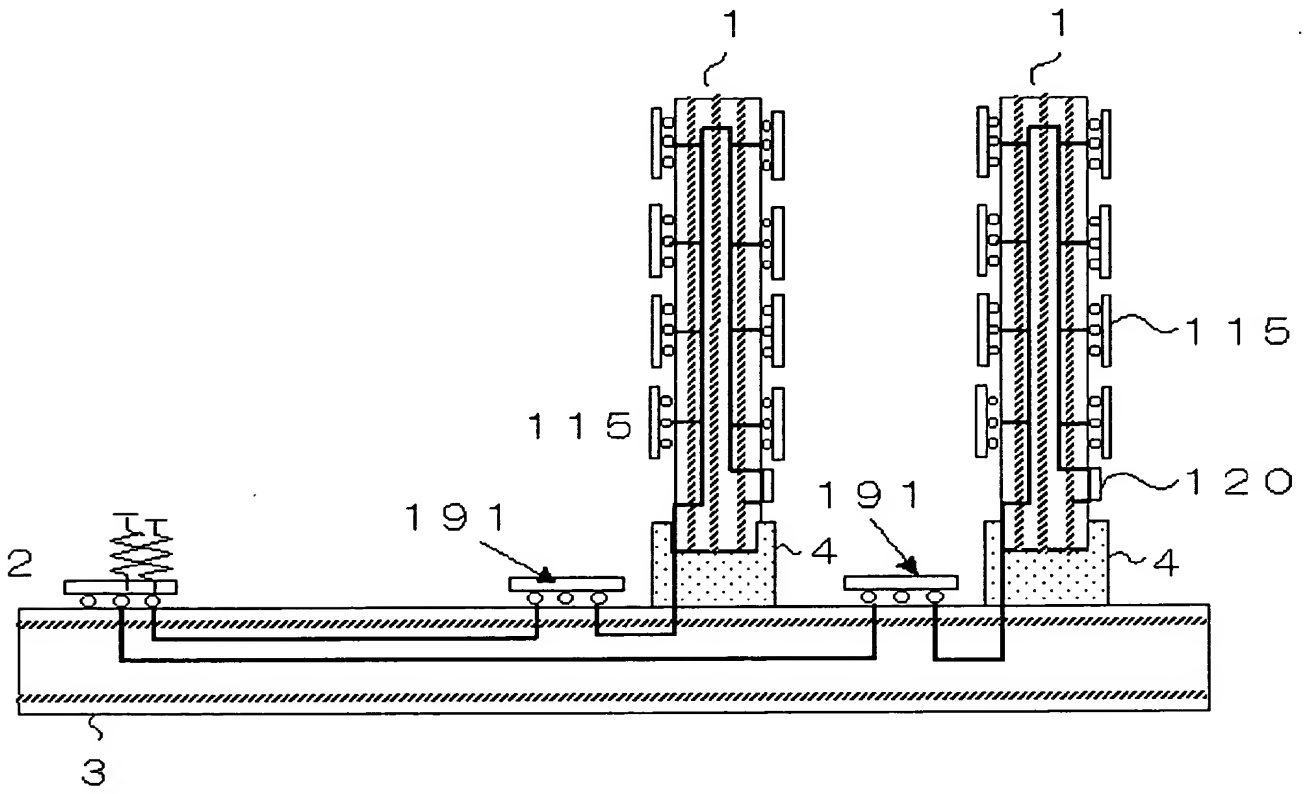


FIG . 19A

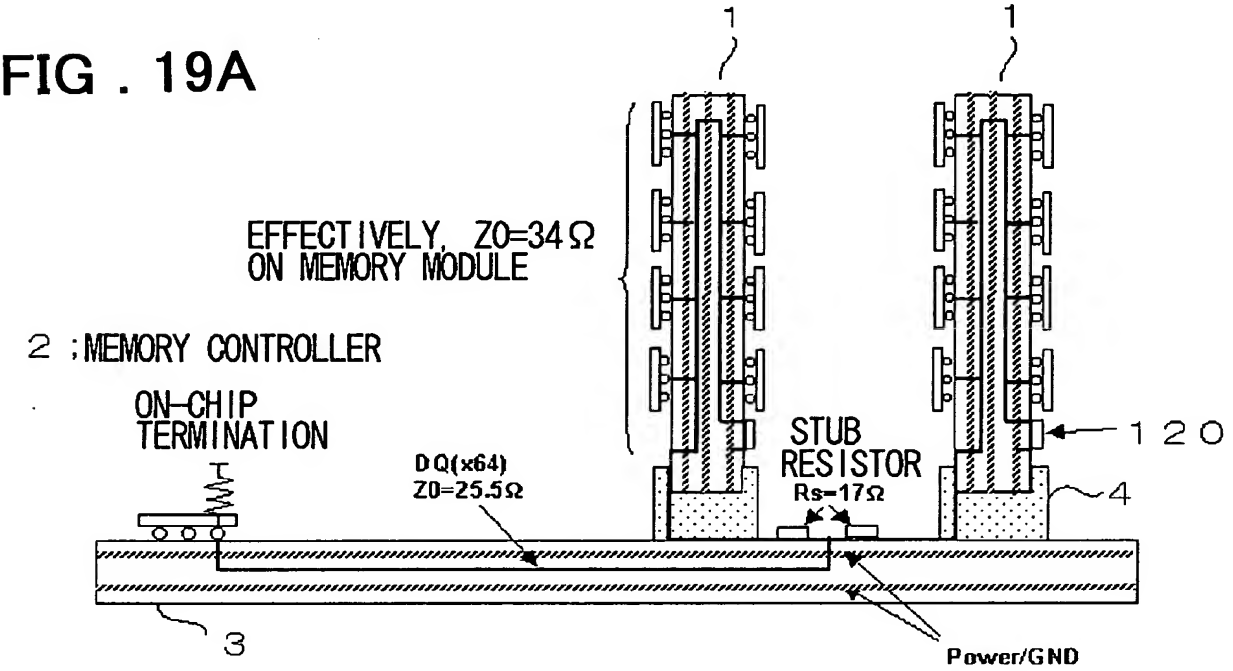
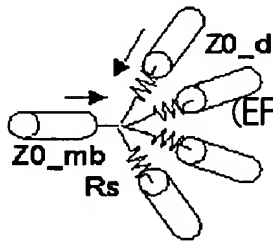


FIG . 19B



N-BRANCH STAR CONNECTION
(EFFECTIVE) Z0 OF MEMORY MODULE = NRS/(N-1)
Z0 OF MOTHERBOARD = (2N-1)RS/N(N-1)

4 BRANCHES

FIG . 20

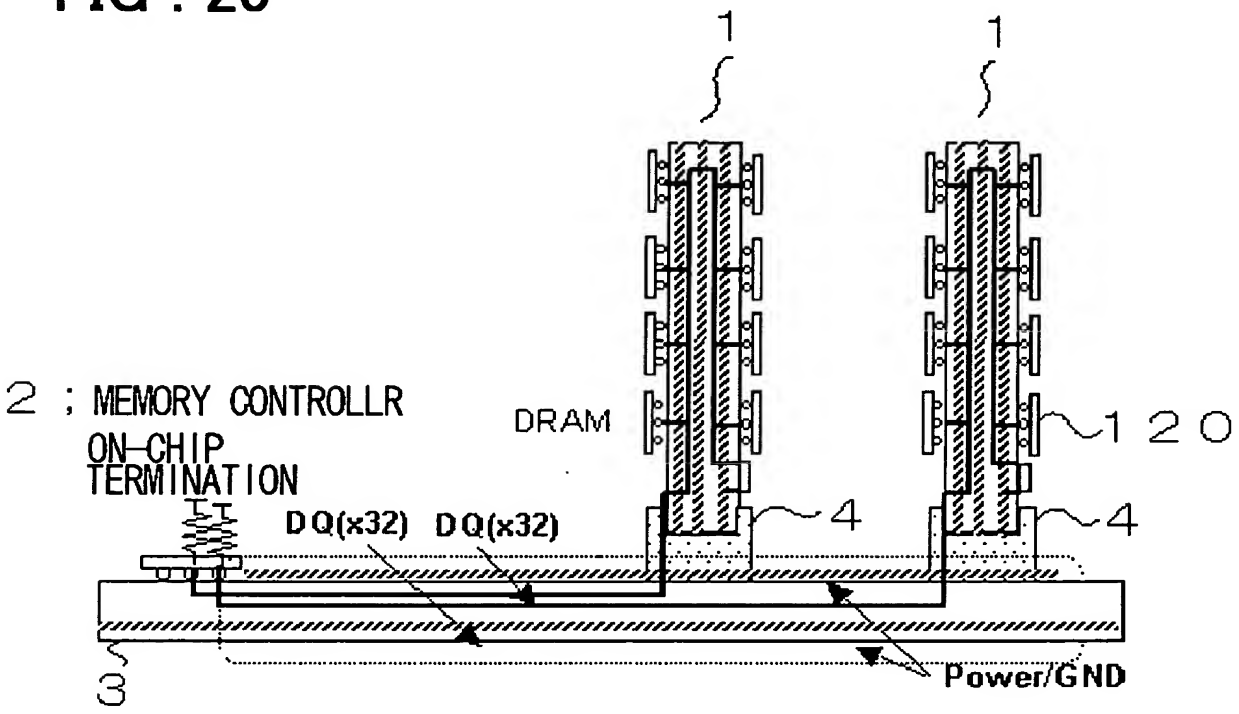

1
1
2 ; MEMORY CONTROLLR
ON-CHIP
TERMINATION
DRAM
120
DQ(x32)
DQ(x32)
4
4
3
Power/GND

FIG . 21A

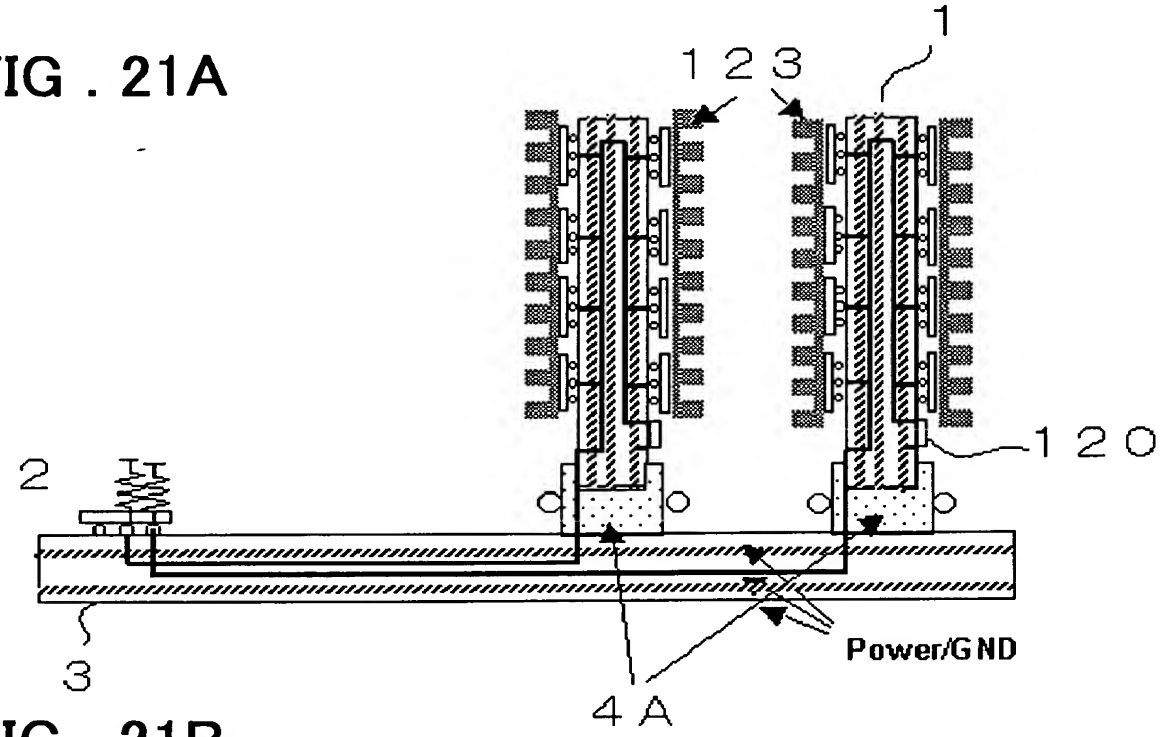


FIG . 21B

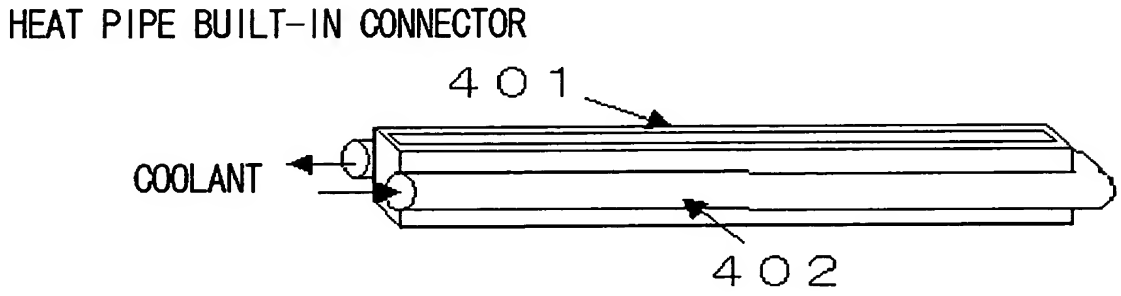


FIG . 22A

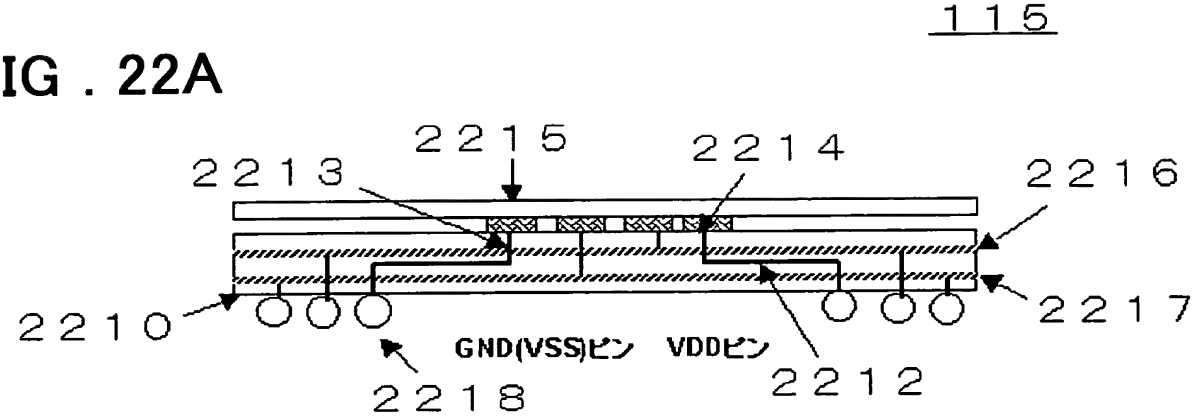


FIG . 22B

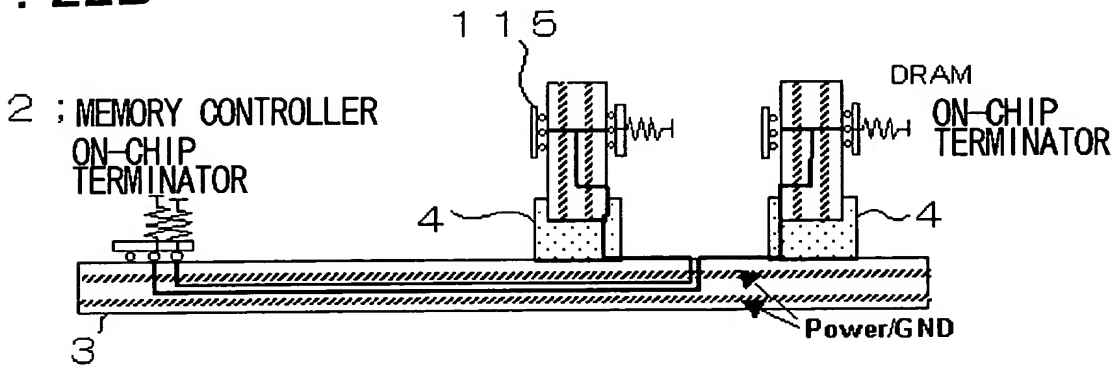


FIG . 23

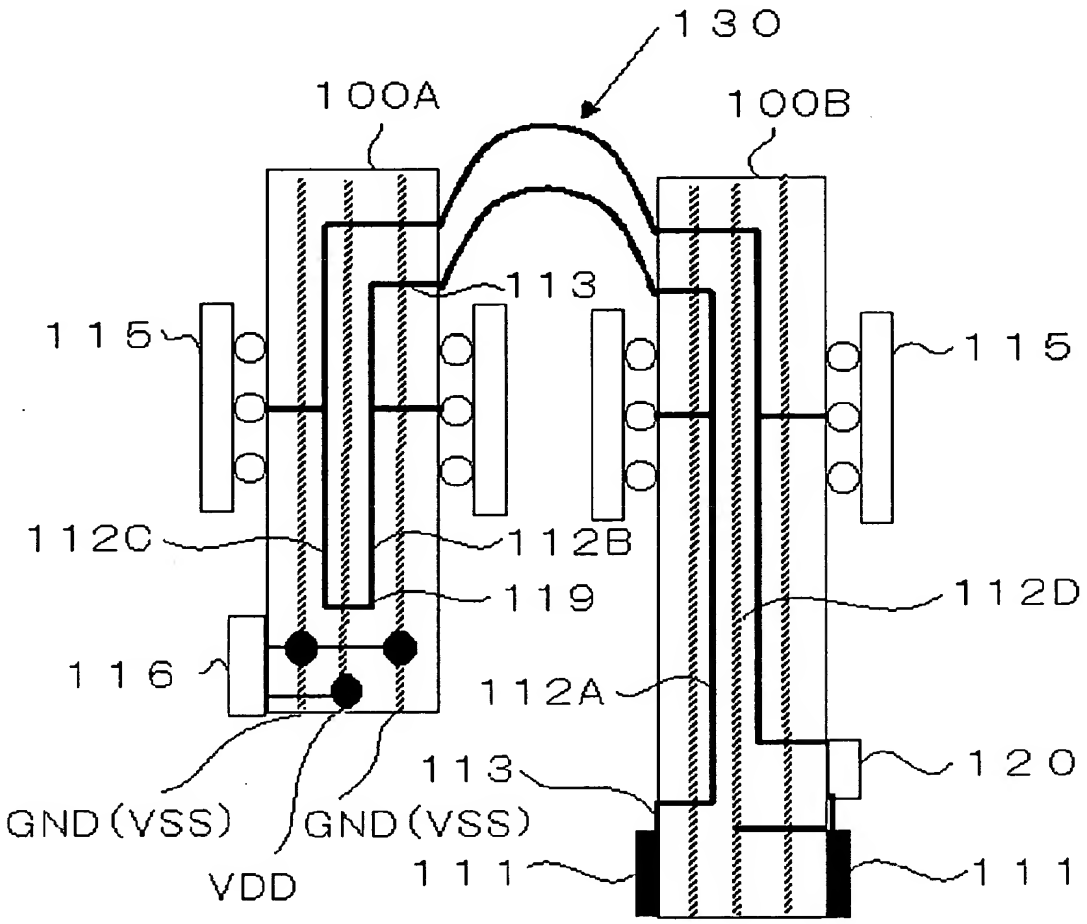

130
100A
100B
113
115
115
112C
112B
119
112D
116
112A
113
120
GND(VSS)
GND(VSS)
VDD
111
111

FIG . 24

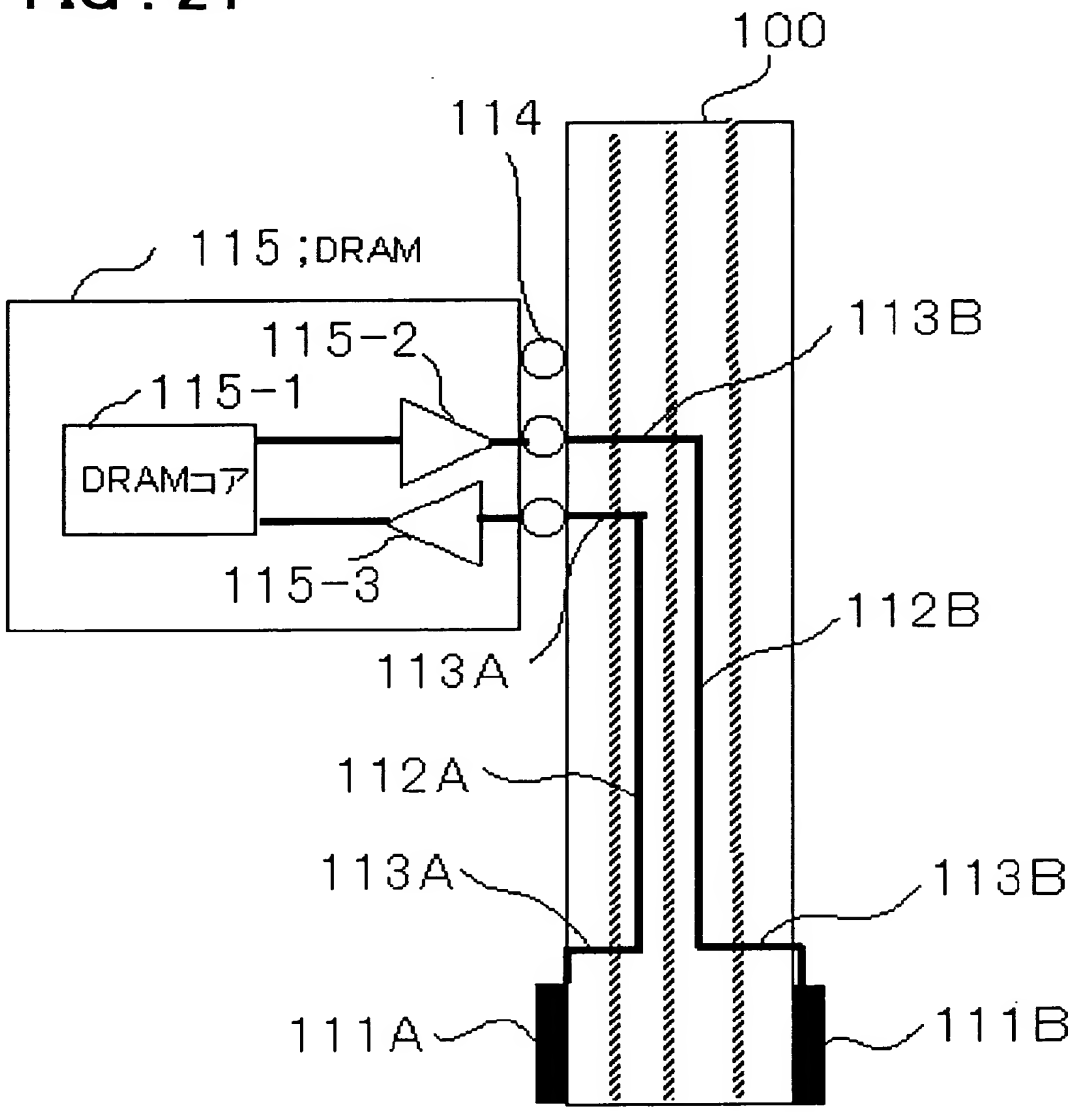

100
114
115 ;DRAM
115-2
113B
115-1
DRAMコア
115-3
113A
112B
112A
113A
113B
111A
111B

FIG . 25

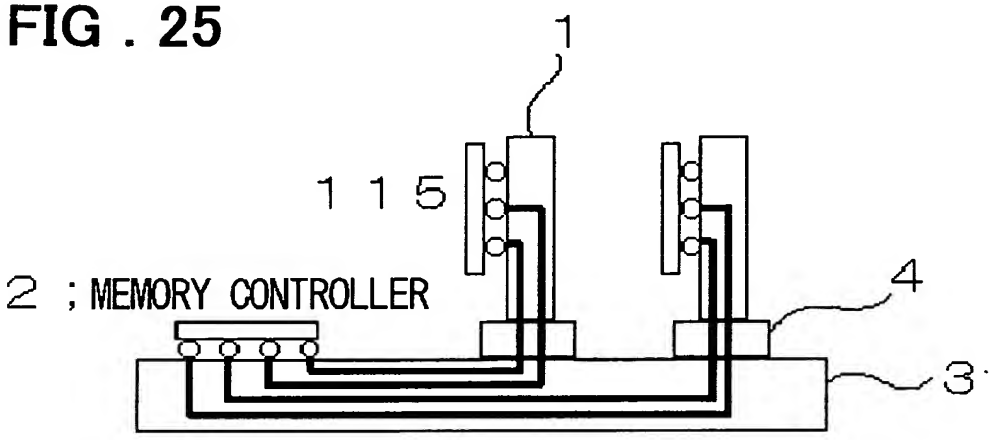


FIG . 26

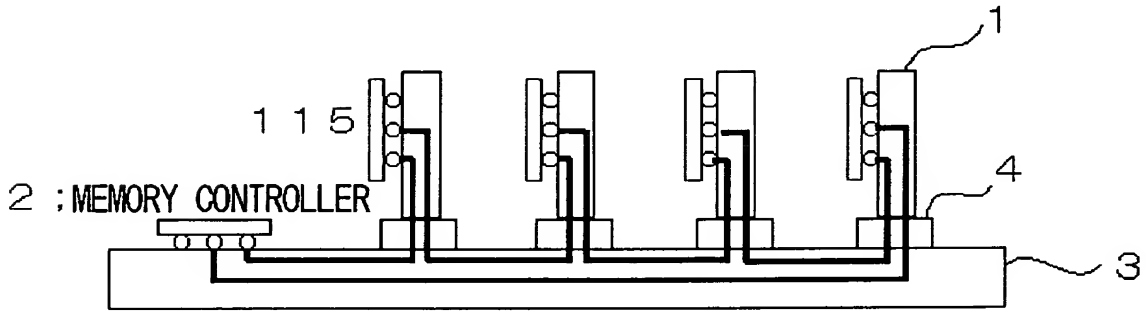


FIG . 27

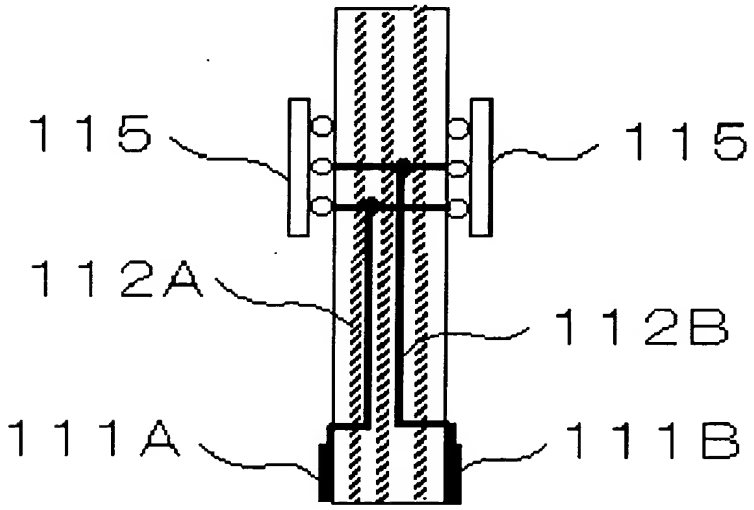


FIG . 28

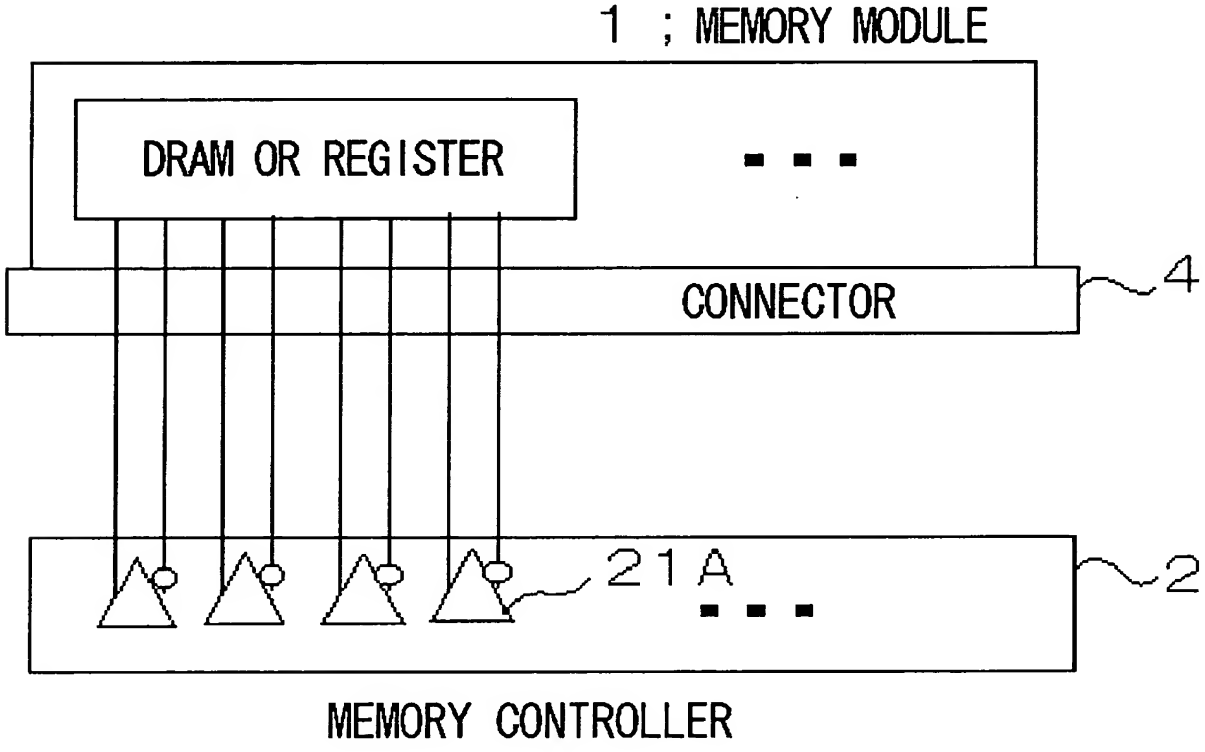

1 ; MEMORY MODULE
DRAM OR REGISTER
CONNECTOR
4
21A
2
MEMORY CONTROLLER

FIG . 29A

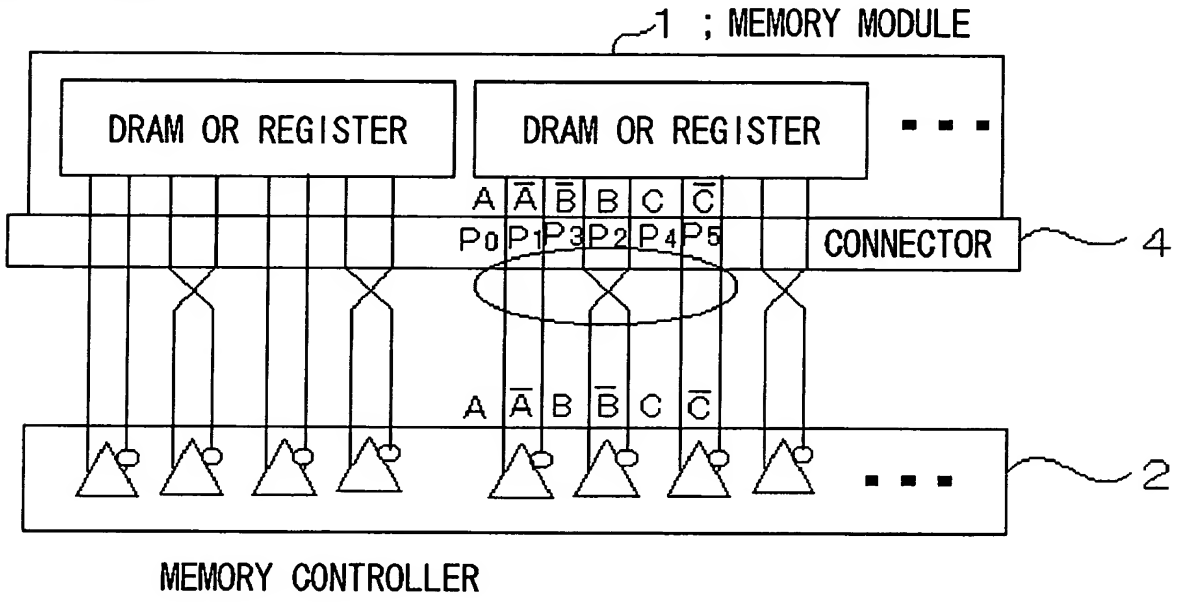


FIG . 29B